REMARKS

I. INTRODUCTION

In response to the Office Action dated September 19, 2006, claim 12 has been canceled without prejudice or waiver, and claims 1-4, 13-17, and 20-22 have been amended. Claims 1-11 and 13-22 remain in the application. Entry of these amendments, and re-consideration of the application, as amended, are respectfully requested.

II. CLAIM AMENDMENTS

Applicants' attorney has made amendments to the claims as indicated above. These amendments were made solely for the purpose of clarifying the language of the claims, and were not required for patentability or to distinguish the claims over the prior art.

III. PRIOR ART REJECTIONS

In paragraph (2) of the Office Action, claims 1-3 and 9-22 were rejected under 35 U.S.C. §102(e) as being anticipated by Oishi et al. (Oishi), U.S. Patent No.6,650,689. In paragraph (3) of the Office Action, claims 4-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Oishi, in view of Nakamura et al. (Nakamura), U.S. Patent No. 6,275,5290.

Applicants respectfully traverse these rejections in light of the amendments above and the arguments below.

The Oishi Reference

Oishi merely describes a correlator and delay lock loop circuit. The present invention reduces the scale of circuitry and shortens the code phase detection time needed to achieve initial synchronization. In a correlator for calculating correlation between a received spreading code contained in a received spread-spectrum signal and a reference spreading code, a combined code generator is included. The combined code generator outputs a combined spreading code by weighting and combining a plurality of phase-shifted reference spreading codes A.sub.1 -A.sub.M. Further, an arithmetic circuit calculates correlation between the received spreading code and the plurality of phase-shifted reference spreading codes simultaneously. A phase detection circuit

detects the phase difference between the received spreading code and a reference spreading code, namely the phase of the received spreading code from the results of the arithmetic operation.

The Nakamura Reference

Similarly, Nakamura merely describes a pseudo-noise generating apparatus. It is also a pseudo-noise generating apparatus capable of starting a pseudo-noise sequence from an arbitrary phase using compact processing circuitry. Tap selection patterns corresponding to a plurality of phase shift amounts are stored in advance in a ROM. By giving a phase shift amount to the ROM and setting the corresponding tap selection pattern in AND gates, the pseudo-noise sequence generated by the pseudo-noise generator is shifted in phase, and is loaded into a shift register. After setting a new phase amount in the ROM, the contents of the shift register are transferred into a shift register in the pseudo-noise generator. By repeating this operation, the desired phase shift is accomplished as a sum of a plurality of phase shift amounts.

The Claims are Patentable over the Cited References

Independent claims 1, 13, and 16 are generally directed to a code phase generator. A generator in accordance with the present invention comprises a shift register comprising N outputs and an input to which a code sequence is applied, N being an integer greater than two, the shift register being controlled by a clock signal; and a plurality of phase delay networks, controlled by a separate clock signal distinct from the clock signal, each phase delay network comprising: a plurality of multipliers, each multiplier receiving an input signal comprising a sequentially delayed code sequence and also receiving an input comprising a control signal; and an adder block, coupled to the output of the plurality of multipliers, wherein the control signals are selected to allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks.

Neither of the cited references teach nor suggest these various elements of Applicants' independent claims. Specifically, the Oishi and Nakamura references do not teach or discuss the limitation of the control signals being selected to allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks, nor do the cited references teach or suggest phase delay networks controlled by a separate clock signal distinct from the clock signal, as recited in the claims of the present invention.

The Oishi reference shows, e.g., in FIG. 3, that each of the sequentially delayed code sequences signals A1-AM reach the adder 22c through the Multipliers MP1-MPn. Further, there is a single clock, e.g., Oscillator 25, that controls the PN generator 21 (along with clock feedback from phase detection circuit 24). See Oishi, FIG. 3.

However, Oishi does not show a separate clock signal, (CLKsr) which controls the phase delay networks, distinct from the clock signal. As discussed above, Oishi does not show a separate clock signal at all, much less one that controls the phase delay network (22a in Oishi FIG. 3) separate from the code generator (reference number 21 in Oishi).

Further, Oishi does not show the control signals that allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks. As shown in FIG. 9A of the present invention, each of the inputs (ec0-ec8, for example) allows only one of the signals from shift register 702 to reach adder 910; for example, ec0-ec7 are a "0" signal, and ec8 is a signal of non-zero value. When the ec0-ec8 signals are multiplied at multipliers 901-909 by the outputs of the shift register 702, only the sequentially delayed signal from rgister 711 reaches adder 910; all other signals are multiplied by zero, and thus do not reach the adder 910.

In Oishi, the weighted coefficients W1-Wm give a combined spreading code A at the output of the Adder 22c, which means that the combined spreading code is a weighted function of at least two, if not all, of the outputs of the shift register 22a. As such, Oishi allows more than one of the sequentially delayed code sequence signals to reach the adder, in direct contradiction with the claims of the present invention, and thus teaches away from the claims of the present invention.

The Nakamura reference does not remedy the deficiencies of the Oishi reference; specifically, Nakamura does not discuss, teach, or suggest the limitations of of the control signals being selected to allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks, nor do the cited references reach or suggest phase delay networks controlled by a separate clock signal distinct from the clock signal, as recited in the claims of the present invention.

The various elements of Applicants' claimed invention together provide operational advantages over the systems disclosed in Oishi and Nakamura. In addition, Applicants' invention

solves problems not recognized by Oishi and Nakamura. For example, and not by way of limitation, the present invention allows for a change in resolution in the tap outputs of the shift register, because the shift register 702 is controlled by a different clock (CLKsr) than the code generator. This allows for better tracking resolution than the Oishi and Nakamura references can achieve. Further, as shown in FIG. 9A, with a separate clock function, the delay network does not have to be contiguous as required by Oishi FIG. 3.

Thus, Applicants submit that independent claims 1, 13, and 16 are allowable over Oishi and Nakamura. Further, dependent claims 2-11, 14, 15, and 17-22 are submitted to be allowable over Oishi and Nakamura in the same manner, because they are dependent on independent claims 1, 13, and 16, respectively, and because they contain all the limitations of the independent claims. In addition, dependent claims 2-11, 14, 15, and 17-22 recite additional novel elements not shown by Oishi and Nakamura.

IV. CONCLUSION

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

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